In the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application.

1. (currently amended) A method of making a wafer scale package for electronic circuits, comprising the steps of:

placing electronic circuits each having at least one electronic device and associated plurality of signal lines comprised of at least one metal layer at respective circuit locations on a base wafer;

forming cavities on ~~the~~ an undersurface of a cover wafer at respective circuit locations to accommodate said respective circuit electronic devices, when said wafers are joined;

forming and metalizing vias in said cover wafer;

applying at least one initial layer of metal in and on an undersurface of said vias and thereby forming via pads;

applying at least one initial layer of metal on a top surface of said base wafer around the periphery of each said location; and

applying at least one initial layer of metal on an undersurface of said cover wafer around the periphery of each said location;

metalizing ~~the~~ a periphery of each said circuit location on said base and cover wafers with at least one intermediate layer of metal;

metalizing an electric contact between ~~the~~ said via pads ~~bottom of a said metalized via~~ and said signal lines with at least one intermediate layer of metal;

wherein the number and thickness of metal layers at the periphery of each said location is substantially equal to the number and thickness of metal layers at said vias and signal lines for ensuring planar alignment of the base and cover wafers when joined together;

joining said base and cover wafers at predetermined pressure, temperature and time conditions to form a peripheral hermetic seal around each said circuit location and a via hermetic seal around each said bottom of ~~a~~ said ~~via~~ vias; and

dicing said joined and sealed wafers along said locations to provide individual die packages.

2. (original) A method of making a wafer scale package according to claim 1 which includes the step of:

providing a base wafer of quartz.

3 (original) A method of making a wafer scale package according to claim 1 which includes the step of:

providing a cover wafer of quartz.

4. (cancelled).

5. (cancelled)

6. (original) A method of making a wafer scale package according to claim 1 which includes the step of:

joining said base and cover wafers at a pressure of around 30 to 80 psi.

7. (original) A method of making a wafer scale package according to claim 1 which includes the step of:

joining said base and cover wafers at a temperature of around 120° C to 200° C.

8. (original) A method of making a wafer scale package according to claim 1 which includes the step of:

joining said base and cover wafers at said predetermined pressure and temperature for around 1 to 3 hours.

9. (new) A method of making a wafer package according to claim 1 wherein said base wafer and said cover wafer are comprised of quartz.

10. (new) A method of making a wafer scale package according to claim 9 wherein said at least one initial layer of metal on the surface of said vias, the top surface of said base wafer and the undersurface of said cover wafer comprises a layer of titanium for enhancing adhesion to said quartz wafers and said vias.

11. (new) A method of making a wafer scale package according to claim 1 wherein said at least one intermediate layer of metal at each said periphery and each of said via pads comprise a plurality of intermediate metal layers including adjacent layers of indium and nickel which fuse so as to become a strength enhancing indium-nickel alloy upon joining said base and cover wafers.

12. (new) A method of making a wafer scale package according to claim 11 and additionally including at least one outer layer of metal adjacent the indium layer and the nickel layer of said intermediate layers.

13. (new) A method of making a wafer scale package according to claim 11 and additionally including an outer layer of metal respectively adjacent the indium layer and the nickel layer of said intermediate layers.

14. (new) A method of making a wafer scale package according to claim 11 wherein the base wafer and cover wafer include at least one additional layer of metal between the respective layers of titanium and said intermediate layers.

15. (new) A method of making a wafer scale package for electronic circuits, comprising the steps of:

placing electronic circuits each having at least one electronic device and associated signal lines at respective circuit locations on a base wafer comprised of quartz;

forming cavities on an undersurface of a cover wafer comprised of quartz at respective circuit locations to accommodate said respective circuit electronic devices, when said wafers are joined;

forming vias in said quartz cover wafer;

applying an initial metal layer of titanium on an inner surface and an undersurface of said vias;

applying an initial metal layer of titanium on the top surface of the quartz base wafer around the periphery of each said location; and

applying an initial metal layer of titanium on the undersurface of the quartz cover wafer around the periphery of each said location;

metallizing a periphery of each said location on said base and cover wafers with a plurality of intermediate metal layers including adjacent layers of indium and nickel;

metallizing an electric contact between a bottom of a said metallized via and said signal lines with a like number of intermediate metal layers also including adjacent layers of indium and nickel;

wherein the number and thickness of metal layers at the periphery of each said location is substantially equal to the number and thickness of metal layers at said vias and signal lines for ensuring planar alignment of the base and cover wafers when joined together;

joining said base and cover wafers at a pressure of about 30 to 80 psi, at a temperature of about 120°C to 200°C and for about 1 to 3 hours to form a peripheral hermetic seal around each said circuit location and a via hermetic seal around each said bottom of said via.

16. (new) A method according to claim 13 and additionally including the step of:

dicing said joined and sealed wafers along said locations to provide individual die packages.